SWU Engineering Journal (2016) 11(1), 50-60
วารสารวิศวกรรมศาสตร์ มหาวิทยาลัยศรีนครินทรวิโรฒ
ปีที่ 11 ฉบับที่ 1 เดือน มกราคม – มิถุนายน พ.ศ. 2559

An Adaptive Combination of Nine-switch Inverter Applications using Level- and Phase-shift Space Vector Duty-cycle Modulations

Neerakorn Jarutus and Yuttana Kumsuwan*
Center of Excellence in Power Conversion Technology, Department of Electrical Engineering,
Faculty of Engineering, Chiang Mai University, Chiang Mai, Thailand, 50200
*Corresponding author: E-mail: yt@eng.cmu.ac.th

ABSTRACT

This paper presents the proposed level-shift and the phase-shift duty-cycle modulations, which are based on the continuous carrier-based space vector pulse width modulation (SVPWM) via the ac and dc components injection technique, for an adaptive combination of nine-switch inverter applications. The dual modulation techniques are selected to overcome the output voltage distortion of the nine-switch inverter caused by the cross-over of the duty-cycle modulating signals, due to its existing shifted phase of the ac component and shifted level of the dc component. The mathematical models of the ac component injection design for the phase-shift technique and the dc component injection design for the proposed level-shift technique were analyzed to carry out the primary drawback avoidance, covering both variable frequency and constant frequency modes. Simulation results are executed on a dominant adjustable speed drive load cooperated with a standalone load to evaluate the dual technique abilities, responding good dynamic- and steady-state performances.

Keyword: Nine-switch inverter, Level-shift duty cycle modulation, Phase-shift duty cycle modulation, Carrier-based space vector pulse width modulation (SVPWM), Cross-over modulation

1. Introduction

Two-level three-phase voltage-source inverters (VSI) are widely used to deliver power from a dc source obtained from a battery, microgrid, renewable energy storages, such as solar photovoltaic and wind or hydro turbine, to a passive or active ac load. Today's two-level VSIs can operate in a wide range of the regulated output voltage and its frequency. Basically, the major advantage of the two-level VSI is its uncomplicated arrangement of the switches and therefore the control strategies are accordingly simple [1]. However, due to its six-switch topology, the stresses on the individual switches are very high because of the basic general VSI requirement of a high dc-bus voltage. Therefore, the multi-level inverters, such as a three-level neutral point clamped VSI [2], are attracted to solve this problem. Even though this inverter type reduces the voltage rating of the switch and affects a further reduction in the electromagnetic interference (EMI), it is the greater number of switches that ultimately leads to an increase in the switching losses and complicated control implementation. Apart from thus, it possibly also results in the dc-bus unbalancing.

To overcome some of the drawbacks of the standard two-level VSI and the existing multi-level inverter issues, a nine-switch converter topology composed of three legs with a series of three switches in each leg was previously introduced in [3] and [4]. It can indeed be an ac-dc-ac converter instead of the rectifier-inverter system [5]-[7] and a dc-ac converter with dual-set output terminals [8]-[11]. Herein, a configuration of the three-phase nine-switch VSI, called nine-switch inverter in short, is especially regarded, as shown in Fig. 1, due to the fact that it independently produces the two symmetrical ac output voltages based on the single output of the two-level VSI. For this reason, the operations of the nine-switch inverter are classified into two modes: 1) constant frequency mode (CF-mode), mostly used in the required constant frequency ac load systems, such as uninterruptible power supplies (UPS) and utility interfaces; and 2) variable frequency mode (VF-mode) that produces the necessary variations in the frequency of the ac output for applications where the speed of an induction motor needs to be regulated, such as an adjustable speed drive (ASD) system. Moreover, the nine-switch inverter can achieve the reduction of the switch components from the multi-level inverters [12] and [13] including a devoid unbalancing of the dc-bus. However, the harmonics of the nine-switch inverter are more than that of the multi-level inverter, due to the increased voltage levels in the multi-level inverter claimed in [14], whereas its quality improvement will depend on the control strategies.

Several alternative control methods have been proposed for the nine-switch inverter. A part of these, a pulse width modulation (PWM) method employs a high-frequency switching technique to give smooth output voltages and reduce the

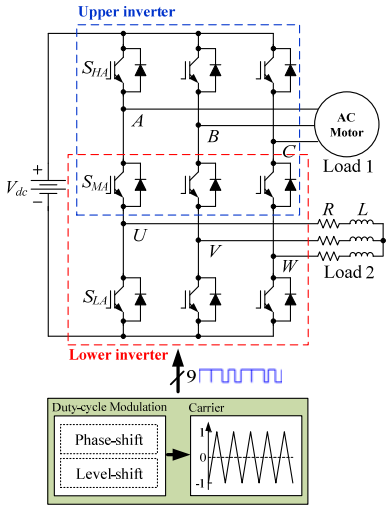


Fig. 1. Nine-switch inverter schematic using level- and phase-shift duty-cycle modulations.

harmonics. A space vector modulation was developed to a 15.5% higher output than that of the sinusoidal PWM (SPWM) [15] and [16]. However, its control ability depends on the arrangement of the switches and the voltage level.

This leads to complications in the generation of switching functions. In order to reduce the control complexity, a carrier-based space vector PWM (SVPWM) was proposed in [17] and [18]. Unfortunately, it needs to inject the ac and dc components for the executed SVPWM method of the nine-switch inverter, leading to some drawbacks with the nine-switch inverter. These are the dc voltage short-circuit, but it is solved by the inserting deadtime into the gate pulses of the switches, and the distortion of the output voltage generated by the cross-over of the duty-cycle modulating signals, due to its existing shifted phase and shifted level of the ac and dc components, respectively.

In this paper, the main focus is to design the injection of the ac and dc components for controlling the duty-cycle modulating signals in order to avoid the major drawback of output voltage distortion. The proposed level-shift technique and the phase-shift technique, for the generation of gate-driven signals,

are selected to solve this problem for both VF- and CF-mode, as shown in Fig. 1. Therefore, the switches operation and the carrier-based SVPWM method of the nine-switch inverter are described in Section 2. And then, the analyzed mathematical modulation for the proposed level-shift technique and the phase-shift technique are performed in Section 3. Section 4 shows the simulation results to verify the dual-modulation techniques by the ASD (for VF-mode) cooperated with the UPS (for CF-mode) operation. Section 5 compares the performances of the dual-modulation techniques to evaluate their feasible attributes. Finally, Section 6 presents the conclusion of this paper.

2. Principle of Nine-switch Inverter Operation

As shown in Fig. 1, the nine-switch inverter is built-up of only nine switches, which is classified into two standard two-level VSIs with three common middle switches. Where the upper and lower inverters are composed of six switches. Considered to each leg, illustrated in phase A, it has three switching states per phase, as listed in Table 1 and shown in Fig. 2. It is evident that two switches of each state are turned on while the other one is turned off. Also, it can be explicitly explained as follows:

State [P] denotes that the top and middle switches are turned on but the bottom switch is turned off. The upper inverter phase voltage v_{AN}, for terminal A respected to negative dc-bus (N), and the lower inverter phase voltage v_{UN}, for terminal U respected to N, equal to the dc-link voltage (V_{dc}).

State [O] denotes that the middle and bottom switches are turned on but the top switch is turned off. It can be seen that the voltages at terminal A and U are directly connected to N. Hence, the phase voltages v_{AN} and v_{UN} are zero.

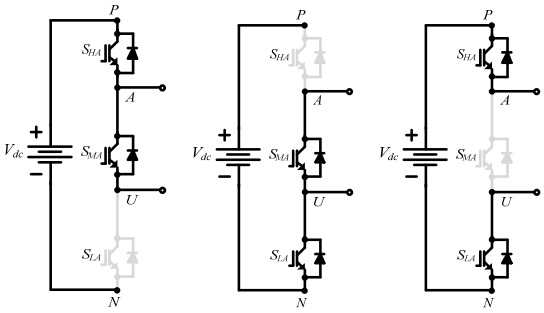


Fig. 2. Schematics description of the switching states for leg A. (a) State [P]. (b) State [O]. (c) State [N].

Table 1. Switching states per phase for leg A of nine-switch inverter

States	Switching-state	On-state	v_{AN}	v_{UV}
[P]	1 1 0	S_{HA}, S_{MA}	V_{dc}	V_{dc}
[O]	0 1 1	S_{MA}, S_{LA}	0	0
[N]	1 0 1	S_{HA}, S_{LA}	V_{dc}	0

State [N] denotes that the top and bottom switches are turned on but the middle switch is turned off. Therefore, the voltage at terminal A is connected to positive dc-bus (P) so that the v_{AN} equals to the V_{dc}. In contrast, the voltage at terminal U is connected to N, leading to the zero in the v_{UN}.

With the switching states per phase for leg A, the switching states for leg B and C are the same configuration as leg A, whereas they will be phase shifted by $-2\pi/3$ and $2\pi/3$ radians, respectively. As a consequence, the nine-switch inverter is characterized by 27 switching mode configurations, as summarized in Fig. 3. Based on the output voltage sequence, it can be divided into eight groups for the upper and lower inverters, as listed in Table 2. Where the zero-mode for the switching states [P P P], [O O O], and [N N N] supply the null line-to-line output voltages of the upper and lower

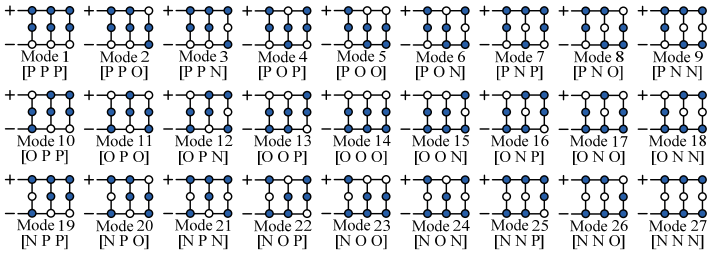


Fig. 3. Switching mode 1 to 27 combination for three-phase leg of the nine-switch inverter.

Table 2. Switching modes of nine-switch inverter

Upper Inverter		
Switching modes	Phase voltage (v_{AN}, v_{BN}, v_{CN})	Line-to-line voltage (v_{AB}, v_{BC}, v_{CA})
1,3,7,9,19,21,25,27	V_{dc}, V_{dc}, V_{dc}	$0, 0, 0$
2,8,20,26	$V_{dc}, V_{dc}, 0$	$0, V_{dc}, -V_{dc}$
4,6,22,24	$V_{dc}, 0, V_{dc}$	$V_{dc}, -V_{dc}, 0$
10,12,16,18	$0, V_{dc}, V_{dc}$	$-V_{dc}, 0, V_{dc}$
5,23	$V_{dc}, 0, 0$	$V_{dc}, 0, -V_{dc}$
11,17	$0, V_{dc}, 0$	$-V_{dc}, V_{dc}, 0$
13,15	$0, 0, V_{dc}$	$0, -V_{dc}, V_{dc}$
14	$0, 0, 0$	$0, 0, 0$

Lower Inverter		
Switching modes	Phase voltage (v_{UN}, v_{VN}, v_{WN})	Line-to-line voltage (v_{UV}, v_{VW}, v_{WU})
1	V_{dc}, V_{dc}, V_{dc}	$0, 0, 0$
2,3	$V_{dc}, V_{dc}, 0$	$0, V_{dc}, -V_{dc}$
4,7	$V_{dc}, 0, V_{dc}$	$V_{dc}, -V_{dc}, 0$
10,19	$0, V_{dc}, V_{dc}$	$-V_{dc}, 0, V_{dc}$
5,6,8,9	$V_{dc}, 0, 0$	$V_{dc}, 0, -V_{dc}$
11,12,20,21	$0, V_{dc}, 0$	$-V_{dc}, V_{dc}, 0$
13,16,22,25	$0, 0, V_{dc}$	$0, -V_{dc}, V_{dc}$
14,15,17,18,23,24,26,27	$0, 0, 0$	$0, 0, 0$

inverters. In addition, it can be observed that there are phase voltages of the upper and lower inverters specified as two output voltage levels, 0 and V_{dc}, on each phase leg. Consequently, the line-to-line voltages identify to the three output voltage levels, $-V_{dc}$, 0, and V_{dc}, which is given by $v_{AB} = v_{AN} - v_{BN}$ (for example).

The nine-switch inverter operating includes of two modes, VF- and CF-mode operations. These operations can be controlled by the carried-based PWM strategy, as shown in Fig. 4 and Fig. 5 (for phase A). The VF-mode PWM control in Fig. 4(a) and 5(a) is established by the variable frequencies and amplitudes of the upper and lower duty-cycle modulating signals, $d^{**}_{MH,A}$ and $d^{**}_{ML,U}$, for the ASD controls of the upper and lower inverters, respectively. For the CF-mode, the frequencies of the upper and lower duty-cycle modulating signals are fixed, as shown in Fig. 4(b) and 5(b). Where the switch signals S_{HA} and S_{LA}, for the top and bottom switches, are generated by the dual duty-cycle modulating signals compared with a high-frequency carrier, and then enter to the exclusive or logically processing to the further switch signal S_{MA} generated for the middle switch. However, the cross-over of the dual duty-cycle signals is a cause of the output voltage distortion, which can be solved by the modulation techniques mentioned in Section 3.

3. Duty-cycle Modulation Schemes

In the nine-switch inverter using the standard continuous space vector duty-cycle modulation, the sinusoidal reference signals are injected by the ac and the dc components. Therefore, the three-phase sinusoidal reference signals $v^{*}_{H,j}$ and $v^{*}_{L,k}$ of the upper and lower space vector duty-cycle

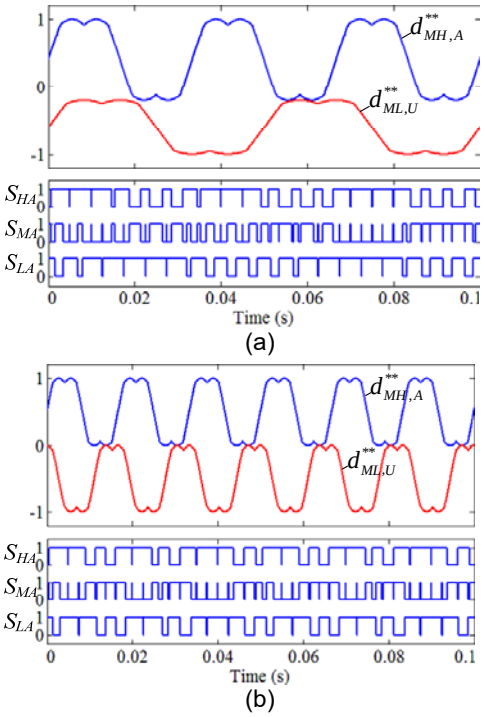


Fig. 4. SVPWM of the phase-shift duty-cycle modulation technique. (a) VF-mode. (b) CF-mode.

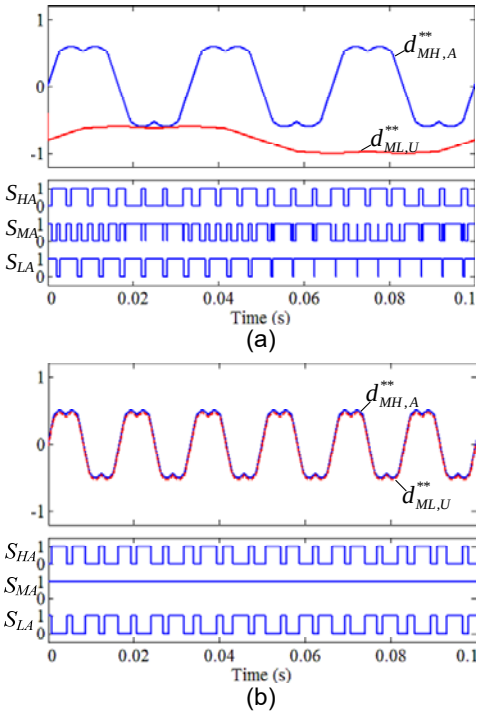


Fig. 5. SVPWM of the level-shift duty-cycle modulation technique. (a) VF-mode. (b) CF-mode.

modulating signals for the upper and lower inverters, respectively, are given as

$$v^{*}_{H,j} = M_H \sin(2\pi f_{H,1} + \theta_j + \phi_H)\,, \tag{1}$$

$$v^{*}_{L,k} = M_L \sin(2\pi f_{L,1} + \theta_k + \phi_L)\,, \tag{2}$$

where M_H, M_L are the modulation indices, $f_{H,1}$, $f_{L,1}$ are the fundamental frequencies, ϕ_H, ϕ_L are the phase-shift angles, θ_j, θ_k are the phase angles (θ_A, $\theta_U = 0$, θ_B, $\theta_V = -2\pi/3$, θ_C, $\theta_W = 2\pi/3$ radians), and $j \in A, B, C$ and $k \in U, V, W$ are the phases to neutral of the three-phase sinusoidal reference signals $v^{*}_{H,j}$ and $v^{*}_{L,k}$, respectively.

The injections $v^{*}_{H,Inj}$ and $v^{*}_{L,Inj}$ for the three-phase sinusoidal reference signals $v^{*}_{H,j}$ and $v^{*}_{L,k}$, respectively, are introduced as

$$v^{*}_{H,Inj} = \overbrace{\left(-\frac{\max(v^{*}_{H,j}) + \min(v^{*}_{H,j})}{2}\right)}^{v^{*}_{H,0}} + \overbrace{\left(1 - M_H \frac{\sqrt{3}}{2}\right)}^{V^{*}_{offset,H}}, \tag{3}$$

$$v^{*}_{L,Inj} = \overbrace{\left(-\frac{\max(v^{*}_{L,k}) + \min(v^{*}_{L,k})}{2}\right)}^{v^{*}_{L,0}} - \overbrace{\left(1 - M_L \frac{\sqrt{3}}{2}\right)}^{V^{*}_{offset,L}}, \tag{4}$$

where $v^{*}_{H,0}$, $v^{*}_{L,0}$ are the ac components, which are the zero-sequence signals, $V^{*}_{offset,H}$, $V^{*}_{offset,L}$ are the dc components, which are the dc offset signals, injected into the $v^{*}_{H,j}$ and $v^{*}_{L,k}$.

Here, the three-phase space vector duty-cycle modulating signals based on time domain are expressed as

$$d^{**}_{MH,j} = v^{*}_{H,j} + v^{*}_{H,Inj}\,, \tag{5}$$

$$d^{**}_{ML,k} = v^{*}_{L,k} + v^{*}_{L,Inj}\,, \tag{6}$$

where $d^{**}_{MH,j}$, $d^{**}_{ML,k}$ are the three-phase upper and lower duty-cycle modulating signals for the upper and lower inverter controls, respectively.

Additionally, the fundamental output voltage of the nine-switch inverter can be obtained by

$$V_{LL,1(rms)} = \frac{\sqrt{6}}{4} M_{H,L} V_{dc}\,, \tag{7}$$

where $V_{LL,1(rms)}$ is the fundamental line-to-line output voltage (rms) of the upper or lower inverter, $M_{H,L}$ is the modulation index of the $d^{**}_{MH,j}$ or $d^{**}_{ML,k}$ in

the linear modulation range of 0 to $2/\sqrt{3}$, which is expanded by 15.5% from the SPWM scheme, within the range of 0 to 1. Specifically, in order to avoid the distortion of the output voltage caused by the cross-over of the $d^{**}_{MH,j}$ and $d^{**}_{ML,k}$, the injections of ac and dc components are then designed.

3.1 Phase-shift Duty-cycle Modulation

In the existing ac components $v^{*}_{H,0}, v^{*}_{L,0}$, the $d^{**}_{MH,j}$ and $d^{**}_{ML,k}$ can possibly be cross-over when the ac components are phase shifted. Therefore, it can be designed on the phase-shift angles constraint, as defined in Table 3. As a consequence, the phase-shift duty-cycle configuration is illustrated in Fig. 4 for both VF- and CF-mode operations.

Table 3. Phase-shift duty-cycle modulation technique

Conditions		Ac component injection design $v^{*}_{H,0}, v^{*}_{L,0}$	
CF-mode	$M_H \neq M_L$	$0° \le \lvert\phi_H - \phi_L\rvert \le 360°$	$M_H + M_L \le 2/\sqrt{3}$
		$\lvert\phi_H - \phi_L\rvert = 0°$	$M_H + M_L > 2/\sqrt{3}$
	$M_H = M_L$	$0° \le \lvert\phi_H - \phi_L\rvert \le 360°$	$M_H = M_L \le 1/\sqrt{3}$
		$\lvert\phi_H - \phi_L\rvert = 0°$	$M_H = M_L > 1/\sqrt{3}$
VF-mode		$M_H + M_L \le 2/\sqrt{3}$	

It can be seen that this technique can avoid the cross-over of the duty-cycle modulating signals for the VF-mode (see Fig. 4(a)) and CF-mode (see Fig. 4(b)); however, its modulation indices are limited. This leads to a further down-scaling of the output voltage of both upper and lower inverters obtained from (7).

3.2 Proposed Level-shift Duty-cycle Modulation

Similarly, as shown in Fig. 5, the proposed level-shift technique is identified to avoid the previously mentioned drawback by regarding the optimal shifting level of the dc components $V^{*}_{offset,H}, V^{*}_{offset,L}$. Therefore, the design level-shift of the dc component injection is expressed in Table 4.

Table 4. Level-shift duty-cycle modulation technique

Conditions		Dc component injection design $V^{*}_{offset,H}, V^{*}_{offset,L}$	
CF-mode	$M_H > M_L$	$V^{*}_{offset,H} = 0$	$0 \le M_H, M_L \le 2/\sqrt{3}$
		$V^{*}_{offset,L} \ge (M_H - M_L)\times(\sqrt{3}/2)$	
	$M_H < M_L$	$V^{*}_{offset,H} \ge (M_L - M_H)\times(\sqrt{3}/2)$	
		$V^{*}_{offset,L} = 0$	
VF-mode	$M_H > M_L$	$V^{*}_{offset,H} = 0$	$M_H + 2M_L \le 2/\sqrt{3}$
		$V^{*}_{offset,L} \ge (M_H + M_L)\times(\sqrt{3}/2)$	
	$M_H < M_L$	$V^{*}_{offset,H} \ge (M_H + M_L)\times(\sqrt{3}/2)$	$2M_H + M_L \le 2/\sqrt{3}$
		$V^{*}_{offset,L} = 0$	

In this technique, the lower modulation index in Fig. 5(a) is half of the phase-shift technique in Fig. 4(a). This is a very low value for the VF-mode. Therefore, it is particularly suitable for the CF-mode, as shown in Fig. 5(b), and the modulation indices of the duty-cycle modulating signals can expand to a higher value than that of the phase-shift technique in Fig. 4(b) without them crossing-over each other, due only to the dc component injection design of this technique. Note that, the higher modulation index is of the regular supply to the inverter for the ASD (VF-mode) and the lower modulation index supply to the inverter with the standalone load for the UPS (CF-mode), as verified in Section 4.

4. Results

The performance of the proposed level-shift duty-cycle modulation in comparison to the phase-shift duty-cycle modulation for the nine-switch inverter was verified using a simulation in the MATLAB/Simulink environment, as the block diagram shown in Fig. 6. The nine-switch inverter was designed for the VF-mode (ASD) cooperated with the CF-mode (UPS) with the rated power at 4.7 kW, the dc-link voltage V_{dc} = 600 V, and the switching frequency f_{sw} = 7.5 kHz. With the ASD,

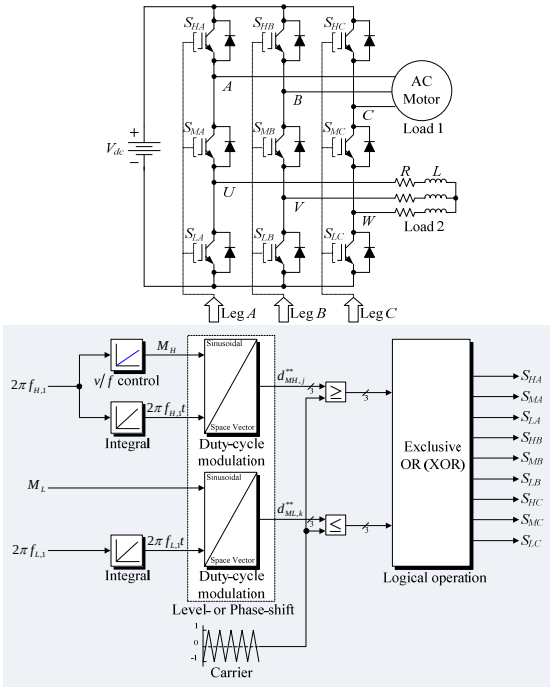


Fig. 6. Nine-switch inverter using the level- and phase-shift techniques block diagram for load 1 with VF-mode and load 2 with CF-mode.

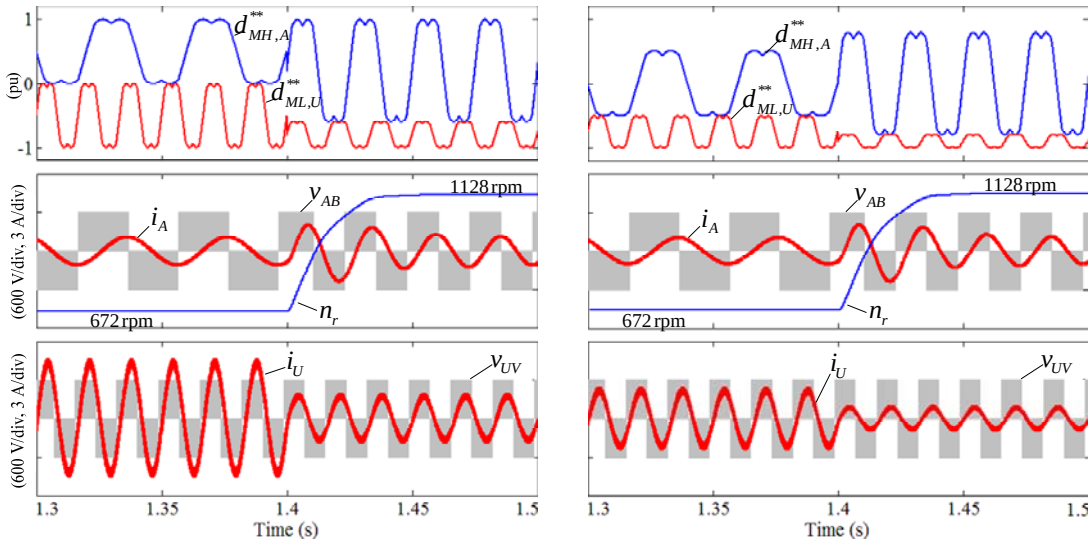
the upper inverter was driven for the induction motor, where its ratings are 1/2 hp, 400 V(rms), 50 Hz, 1.05 A(rms), 2.6 $\mathrm{N\cdot m}$, 1360 rpm and its parameters are set as shown in Table 5, using the standard open-loop v/f control. With the UPS for 208 V(rms), 60 Hz, the lower inverter was connected to the standalone inductive load Z = 40+*j*7.54 Ω.

Simulation results of the phase-shift duty-cycle modulation are shown in Fig. 7(a), 8(a), and 9(a). Fig. 7(a) shows the dynamic outputs responses of the upper and lower inverters. In terms of the duty-cycle modulating signals for the upper and lower inverters ($d^{**}_{MH,A}$ and $d^{**}_{ML,U}$), for the top, the frequency $f_{H,1}$ of the upper duty-cycle modulating signal ($d^{**}_{MH,A}$) is increased by a step command, whereas the frequency $f_{L,1}$ of the lower duty-cycle modulating signal ($d^{**}_{ML,U}$) is kept constant at 60 H. For the upper inverter's output, in the middle,

Table 5. Induction motor parameters

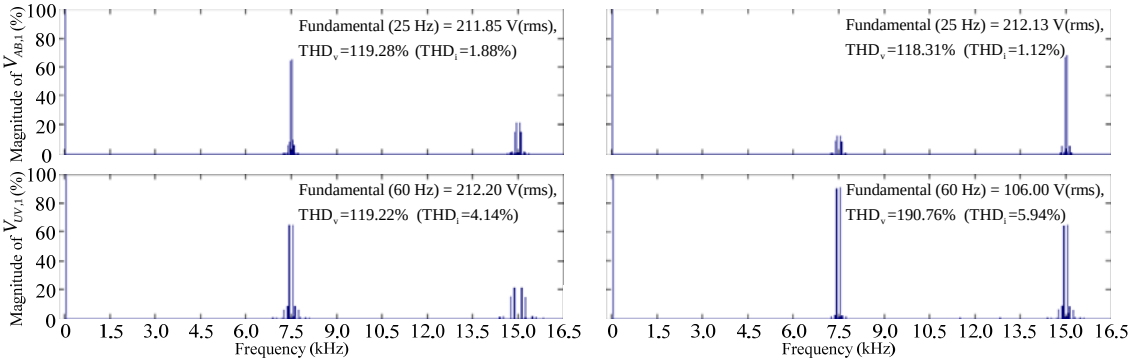
Motor Parameters		Values	
Stator winding resistance	(R_s)	30	Ω
Rotor winding resistance	(R_r)	31.49	Ω
Stator leakage inductance	(L_{ls})	0.0942	H
Rotor leakage inductance	(L_{lr})	0.0942	H
Magnetizing inductance	(L_m)	1	H
Moment of inertia	(J)	0.0028	$\mathrm{kg\cdot m^2}$

the fundamental frequency $f_{H,1}$ is initially 25 Hz and it is stepped to 40 Hz at 1.4 sec, according to the $d^{**}_{MH,A}$. Therefore, the rotor speed (n_r) is brought from 672 rpm to 1128 rpm with a constant load torque. It is obvious that the phase current i_A has a smooth transition and a constant magnitude in steady-state, due to a keeping motor flux constant of v/f control. Accordingly, the output response of the lower inverter, for the bottom, keeps its fundamental frequency $f_{L,1}$ constant at 60 Hz while the magnitude of the phase current i_U is stepped down at 1.4 sec according to a high-speed motor control of the upper inverter. During a steady-state of the $f_{H,1}$ at 25 Hz, the harmonics in the line-to-line output voltage of the upper inverter (v_{AB}) are the same manner as the line-to-line output voltage of the lower inverter (v_{UV}), as shown in Fig. 8(a), whereas the bandwidth of the v_{AB} is narrower than that of the v_{UV}. As the same modulation indices of the $d^{**}_{MH,A}$ and $d^{**}_{ML,U}$ (M_H = M_L = 0.577), the fundamental output voltage components and the $\mathrm{THD_v}$ of the v_{AB} and v_{UV} are identical. It is evident that the lower inverter is suitable for 208 V(rms), 60 Hz system. On the other hand, in the period when the $f_{H,1}$ is 40 Hz, the fundamental output voltage $V_{UV,1}$ decreases to 84.92 V(rms) and its $\mathrm{THD_v}$ is around 216.18% due to a further reduction in the M_L, as shown in Fig. 9(a).



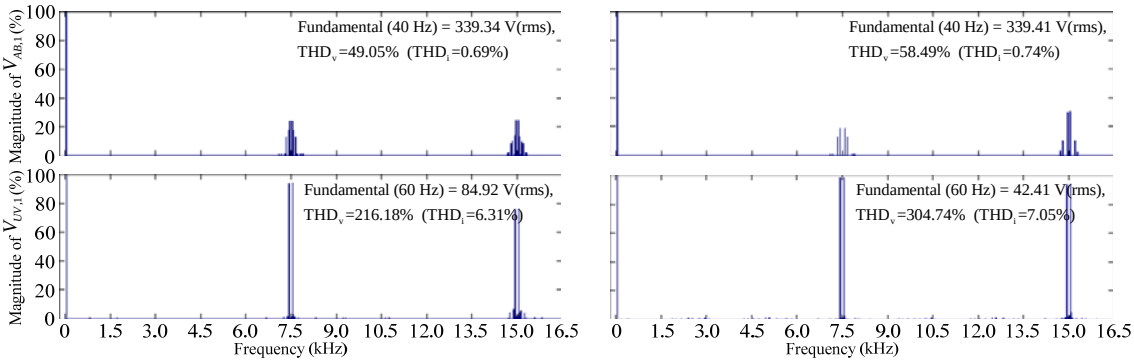
(a) Phase-shift duty-cycle modulation (b) Level-shift duty-cycle modulation

Fig. 7. Simulation results for dynamic output responses of the upper and lower inverters with the open-loop v/f control for the frequency variation of the upper duty-cycle modulating signal ($f_{H,1}$) from 25 Hz to 40 Hz and the constant frequency of the lower duty-cycle modulating signal ($f_{L,1}$) at 60 Hz.



(a) Phase-shift duty-cycle modulation (b) Level-shift duty-cycle modulation

Fig. 8. Simulation harmonic content for the line-to-line output voltages in the steady-state of the upper and lower inverters in the period of the fundamental frequency of the upper inverter output ($f_{H,1}$) is 25 Hz, during the fundamental frequency of the lower inverter output ($f_{L,1}$) at 60 Hz.



(a) Phase-shift duty-cycle modulation (b) Level-shift duty-cycle modulation

Fig. 9. Simulation harmonic content for the line-to-line output voltages in the steady-state of the upper and lower inverters in the period of the fundamental frequency of the upper inverter output ($f_{H,1}$) is 40 Hz, during the constant fundamental frequency of the lower inverter output ($f_{L,1}$) at 60 Hz.

Resulting in the proposed level-shift technique as shown in Fig. 7(b), the $d^{**}_{MH,A}$ appears centrally as a typical space vector duty-cycle without the dc offset ($V_{offset,H}$ = 0) and its frequency $f_{H,1}$ variation is the same condition as the phase-shift case. Since this technique, the modulation index of the $d^{**}_{ML,U}$ is reduced to half of the phase-shift technique. Consequently, the outputs of the upper and lower inverters have the same dynamic responses as shown in Fig. 7(a), except that the phase current i_U magnitude decreases to one-half. In a steady-state for interval of the $f_{H,1}$ is 25 Hz, the fundamental output voltage $V_{AB,1}$ and the $\mathrm{THD_v}$ resultants of the v_{AB} in Fig. 8(b) are identical to that of Fig. 8(a). However, the high-order harmonics at $m_f \pm 1$ and $2m_f \pm 2$ are eliminated. This leads to a slight better quality of the phase current i_A compared with the phase-shift technique, with the same load inductance filter. For the v_{UV} of the lower inverter, the fundamental output voltage $V_{UV,1}$ reduces from Fig. 8(a) to 106.00 V(rms) and its $\mathrm{THD_v}$ is increased to 190.76%. Then, with the high-speed motor control (Fig. 9(b)), the fundamental output voltage $V_{UV,1}$ is only 42.41 V(rms), which is a half of that in Fig. 9(a).

Note that, dual modulation techniques can achieve the stable output voltage and good accordance to the theoretical principle, whereas the lower inverter results in a very low output voltage for the standalone load along with the high-speed motor control of the upper inverter. It is the only drawback of dual techniques for this application. However, this can be solved by boosting the dc-link voltage (V_{dc}), as presented in [19].

5. Comparison of Duty-cycle Modulation Schemes

Subsequently, in order to evaluate the performances of the proposed level-shift technique and the phase-shift technique, a comparison between both methods is introduced in Table 6. In terms of the upper inverter for the ASD, it points out that the dual-modulation techniques results are almost similar at both low-speed (n_r = 672 rpm) and high-speed (n_r = 1128 rpm) motor controls, unless the current harmonic content obtained by the proposed technique at a low-speed control would be slightly better than that of the phase-shift technique. However, it is opposite for a high-speed control. In fact, the motor current is close to sinusoidal waveform so that it is of insignificant attractiveness. With the lower inverter for a UPS, the proposed level-shift modulation provides the lower fundamental output voltage $V_{UV,1}$ of 50% compared to the phase-shift technique. Beyond this, the dual techniques display the very low output voltage $V_{UV,1}$ at high-speed motor control by the upper inverter.

Table 6. Comparison results of level- and phase-shift techniques

Comparison	Low-speed n_r = 672 rpm		High-speed n_r = 1128 rpm	
	Phase-shift	Level-shift	Phase-shift	Level-shift
$V_{AB,1}$ (V(rms))	211.85	212.13	339.34	339.41
$\mathrm{THD_v}$ of v_{AB}	119.28%	118.31%	49.05%	58.49%
$\mathrm{THD_i}$ of i_A	1.88%	1.12%	0.69%	0.74%
$V_{UV,1}$ (V(rms))	212.20*	106.00	84.92*	42.41
$\mathrm{THD_v}$ of v_{UV}	119.22%*	190.76%	216.18%*	304.74%
$\mathrm{THD_i}$ of i_U	4.14%*	5.94%	6.31%*	7.05%

*Better object

Based on the comparison analysis of dual-modulation performances given in this section, the features and drawback for the phase-shift and the proposed level-shift duty-cycle modulations with the proposed application are summarized in Table 7. It can be confirm that the dual-modulation techniques for the upper inverter are in a good performance agreement for ASD in an induction motor. For the lower inverter, the phase-shift technique is available

Table 7. Attributes of level- and phase-shift techniques

Features		Phase-shift	Level-shift
Designed definition		Ac component	Dc component
ASD for upper inverter	$n_r \leq 672$ rpm	✓	✓
	$n_r > 672$ rpm	✓	✓
UPS (208 V, 60 Hz) for lower inverter	$n_r \leq 672$ rpm	✓	×
	$n_r > 672$ rpm	×	×

✓ = Feasible. × = Unfeasible

for the UPS in 208 V, 60 Hz system with the low-speed motor drive ($n_r \leq$ 672 rpm) of the employed 600 V dc-link voltage. Here, it can be observed that the proposed level-shift performance is unfeasible. Furthermore, it is unworkable with high-speed motor drive ($n_r >$ 672 rpm) for the dual techniques. However, it can boost the dc-link voltage for a higher output voltage, especially as the proposed level-shift technique, which requires twice as much as the phase-shift technique.

6. Conclusion

In this paper, the proposed level-shift duty-cycle modulation and the phase-shift duty-cycle modulation, using the standard continuous SVPWM algorithm applied to the nine-switch inverter, have been presented and compared for an adaptive combination of nine-switch inverter applications. An integrated dual control strategy was synthesized based on the mathematical analysis of the ac component design for the phase-shift technique and the dc component design for the proposed technique to prevent the cross-over of the duty-cycle signals, which effects to the output voltage distortion. As a result, the ASD for upper inverter obtained by the dual techniques achieve good dynamic response to regulate from low-speed to high-speed by an open-loop v/f control. With the standalone load for lower inverter, the phase-shift technique is suitable for a UPS of 208 V, 60 Hz system for low-speed control of the upper inverter and the 600 V dc voltage while the proposed technique resulted in 50% less than that of the phase-shift technique. In fact, this leads to the very low output voltage obtained from the dual techniques for the high-speed control, but it can be increased by boosting the dc voltage.

7. Acknowledgment

This work is supported by the graduate school, Chiang Mai University.

8. References

[1] M. Wei, L. P. Chiang, and D. Yi. “Optimal design of two level inverters”. *IEEE-IPEC*. 27-29/Oct./2010. Suntec Singapore International Convention & Exhibition Centre Singapore, Singapore: pp. 705-710.

[2] K. Lavanya and V. Rangavalli, “A novel technique for simulation & analysis of SVPWM two & three-level inverters,” *IJERA Journal*, vol. 3, pp. 455-460, Sep.-Oct. 2013.

[3] C. Liu, B. Wu, and N. R. Zagari, “Ac-to-ac (frequency) converter with three switches per leg,” U.S. Patent 7 310 254, 2007.

[4] T. Kominami and Y. Fujimoto. “A novel nine-switch inverter for independent control of two three-phase loads”. *IEEE-IAS*. 23-27/Sep./2007. Louisiana, USA: pp. 2346-2350.

[5] C. Liu, B. Wu, N. R. Zargari, D. Xu, and J. Wang, “A novel three-phase three-leg ac/ac converter using nine IGBTs,” *IEEE Trans. Power Electron.*, vol. 24, pp. 1151-1160, May 2009.

[6] C. Liu, B. Wu, N. Zargari, D. Xu, and J. Wang, “Novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications,” *EPE Journal*, vol. 19, pp. 1-9, Jun. 2009.

[7] L. Zhang, P. C. Loh, and F. Gao, “An integrated nine-switch power conditioner for power quality enhancement and voltage sag mitigation,” *IEEE Trans. Power Electron.*, vol. 27, pp. 1177-1190, Mar. 2012.

[8] S. M. Dehghan, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, “A dual-input-dual-output z-source inverter,” *IEEE Trans. Power Electron.*, vol. 25, pp. 360-368, Feb. 2010.

[9] S. M. Dehghan, M. Mohamadian, and A. Yazdian, “Hybrid electric vehicle based on bidirectional z-source nine-switch inverter,” *IEEE Trans. Veh. Technology*, vol. 59, pp. 2641-2653, Jul. 2010.

[10] X. Liu, P. Wang, P. C. Loh, and F. Blaabjerg, “A compact three-phase single-input/dual-output matrix converter,” *IEEE Trans. Ind. Electron.*, vol. 59, pp. 6-16, Jan. 2012.

[11] X. Liu, P. Wang, P. C. Loh, and F. Blaabjerg, “A three-phase dual-input matrix converter for grid integration of two ac type energy resources,” *IEEE Trans. Ind. Electron.*, vol. 60, pp. 20-30, Jan. 2013.

[12] Z. Qin, P. C. Loh, A. S. Bahman, and F. Blaabjerg, “Evaluation of current stresses in nine-switch energy conversion systems,” *IET Power Electron.*, vol. 7, pp. 2877-2886, May 2014.

[13] Z. Qin, P. C. Loh, and F. Blaabjerg, “Application criteria for nine-switch power conversion systems with improved thermal performance,” *IEEE Trans. Power Electron.*, vol. 30, pp. 4608-4620, Aug. 2015.

[14] T. Prathiba and P. Renuga, “A comparative study of total harmonic distortion in multi level inverter topologies,” *IISTE Journal*, vol. 2, pp. 26-36, 2012.

[15] S. M. D. Dehnavi, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh, “Space vector modulation for nine-switch converters,” *IEEE Trans. Power Electron.*, vol. 25, pp. 1488-1496, Jun. 2010.

[16] S. M. Dehghan, A. Amiri, M. Mohamadian, and M. A.E. Andersen, “Modular space-vector pulse-width modulation for nine-switch converters,” *IET Power Electron.*, vol. 6, pp. 457-467, Dec. 2013.

[17] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang, and H. Gao, “Optimal pulsewidth modulation of nine-switch converter,” *IEEE Trans. Power Electron.*, vol. 25, pp. 2331-2343, Sep. 2010.

[18] F. C. de Andrade, F. Bradaschia, L. R. Limongi, and M. C. Cavalcanti. “A generalized scalar pulse-width modulation for nine-switch inverters with maximum amplitude constant frequency operation mode”. *IEEE-ISIE*. 3-5/Jun./2015. Rio de Janeiro, Brazil: pp. 160-165.

[19] S. M. Dehghan, M. Mohamadian, A. Yazdian, and F. Ashrafzadeh. “Dual-input dual-output z-source inverter”. *IEEE-ECCE*. 20-24/Sep./2009. CA, USA: pp. 3668-3674.